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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
10/064,524	07/24/2002	Jie Wei Chin	MTKP0026USA	6627

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER
NGUYEN, DILINH P

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)
10/064 514	CHO ET AL
Examiner	**Art Unit**
DiLanh Nguyen	2814

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1 ☐ Certified copies of the priority documents have been received.

2 ☐ Certified copies of the priority documents have been received in Application No. _____.

3 ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1 ☒ Notice of References Cited, PTO-892
2 ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
3 ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s).
4 ☐ Interview Summary, PTO-413, Paper No(s).
5 ☐ Notice of Informal Patent Application, PTO-152
6 ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 8-9, 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (U.S. Pat. 5349239) in view of Li (U.S. Pat. 5696466).

- Regarding claims 1 and 13, Sato discloses a semiconductor device (fig. 3, column 3, lines 65 et seq.) comprising:

  a substrate 10;

  a heat sink 4 for dissipating heat;

  a transistor disposed on the substrate, the transistor comprising a collector 8, a base 7 and at least an emitter 5.

  Sato fails to disclose an emitter electrode directly connecting the heat sink and the emitter.

  Li discloses a semiconductor (fig. 5) comprising:

  a transistor comprising a collector, a base and an emitter;

  a heat sink 404 for dissipating heat (column 2, lines 8-12 and column 8, lines 11-12).

  an emitter electrode 405 directly connecting the heat sink and the emitter

Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to modify the device of Sato to provide a precision of the impedance matching and reduce the manufacturing and packaging costs but also improve device performance, as shown by Li.

- Regarding claim 2, Sato discloses the transistor is a hetero bipolar transistor HBT (column 6, lines 50-53).
- Regarding claim 3, Li discloses the emitter comprises a metallization layer 406.
- Regarding claim 4, Li discloses the emitter electrode is a bump (column 5, line 64) and Sato discloses the bump electrode 1 (column 4, line 10).
- Regarding claim 5, Sato discloses the substrate and the heat sink sandwich the transistor.
- Regarding claim 8, Sato discloses the device comprising more than one emitter 5 and 5a, and emitters are mutually connected by a metallization layer.
- Regarding claims 9 and 15, Li discloses the emitter electrode and the heat sink provide an electrical ground connection to the emitter (abstract and column 8, lines 11-12).
- Regarding claims 11 and 16, Sato discloses a plurality of transistors and a plurality of emitter electrodes are disposed in an array, and operate as a functional device.
- Regarding claim 12, Sato discloses the substrate 10 is a GaAs substrate (column 4, lines 61).

- Regarding claim 14, Sato discloses disposing a metallization layer 5 on the substrate 10 to form the emitter, and disposing a second metallization layer 3 to mutually connect emitters 5 and 5a.

3. Claims 1, 6-7, 10, 13 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirakawa (EP 1077494) in view of Li (U.S. Pat. 5696466).

- Regarding claims 1, 13 and 17, Shirakawa discloses a semiconductor device (fig. 1B) comprising:

a substrate 13;

an electrically conductive layer 12 (column 10, line 36); and

a transistor 50 disposed on the substrate, the transistor including a collector 3, a base 2 and an emitter 1;

Shirakawa fails to disclose a bump directly disposed on the emitter so as to connect the emitter with the electrically conductive layer for heat dissipation.

Li discloses a semiconductor (fig. 5) comprising:

a transistor comprising a collector, a base and an emitter;

a heat sink 404 for dissipating heat (column 2, lines 8-12 and column 8, lines 11-12);

a bump 405 (column 5, lines 64) directly disposed on the emitter so as to connect the emitter with the heat sink for heat dissipation. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Shirakawa to provide a precision of the impedance matching and

reduce the manufacturing and packaging costs but also improve device performance, as shown by Li.

- Regarding claim 6, Shirakawa discloses the emitter electrode 1 is a backside via penetrating the substrate 13.
- Regarding claim 7, Shirakawa discloses the heat sink 12 and the transistor 50 sandwich the substrate.
- Regarding claim 10, Shirakawa discloses the heat sink 12 is a metal layer (column 10, line 36).
- Regarding claim 18, Li discloses the heat sink 404 and the substrate (the layer that the emitter, base and collector disposed on) sandwich the transistor.
- Regarding claim 19, Li discloses the heat sink provides an electrical ground connection for to the emitter (column 8, lines 11-12).
- Regarding claim 20, Shirakawa discloses the electrical conductive layer 12 is a metal layer (column 10, line 36).

4 Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (U.S. Pat. 5349239) in view of Li (U.S. Pat. 5696466).

Sato discloses a semiconductor device (fig. 3, column 3, lines 65 et seq.) comprising,

a substrate 10,

a heat sink 4 for dissipating heat.

a transistor disposed on the substrate, the transistor comprising a collector 8, a base 7 and an emitter 5, the emitter including an enlarged portion located laterally away from the collector and the base.

Sato fails to disclose an emitter electrode directly connecting the heat sink and the emitter.

Li discloses a semiconductor (fig. 5) comprising:

a transistor comprising a collector, a base and an emitter;

a heat sink 404 for dissipating heat (column 2, lines 8-12 and column 8, lines 11-12);

a flip chip bump 405 (column 5, line 64) directly connecting the heat sink and the emitter. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Sato to provide a precision of the impedance matching and reduce the manufacturing and packaging costs but also improve device performance, as shown by Li.

- Regarding claim 22, Li discloses the flip chip bump and the heat sink provide an electrical ground connection to the emitter (abstract and column 8, lines 11-12).

Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirakawa (EP 1077494) in view of Sato (U.S. Pat. 5349239).

Shirakawa discloses a semiconductor device (fig. 1B) comprising

a substrate 13

a transistor 50 disposed on the substrate, the transistor including a collector 3, a base 2 and an emitter 1;

a heat sink 12 for dissipating heat; and

a via 10 connecting the heat sink and the emitter, the via penetrating the substrate at the location of the emitter.

Shirakawa fails to disclose the emitter including an enlarged portion located laterally away from the collector and the base.

Sato discloses a semiconductor device (fig. 3) comprising:

a substrate 10;

a transistor disposed on the substrate, the transistor including a collector 8, a base 7 and an emitter 5, the emitter including an enlarged portion located laterally away from the collector and the base. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Shirakawa to reduce the inductance of the outgoing line, as shown by Sato.

- Regarding claim 24, Shirakawa discloses the via and the heat sink provide an electrical ground connection to the emitter.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (703) 305-6983. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DLN
July 22, 2003